IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Dewitt, Jr. et al.**	§	
	§	Group Art Unit: **2183**
Serial No. **10,675,831**	§	
	§	Examiner: **Johnson, Brian P.**
Filed: **September 30, 2003**	§	
	§	
For: **Method and Apparatus for Generating Interrupts Upon Execution of Marked Instructions and Upon Access to Marked Memory Locations in a Data Processing System**	§	

Commissioner for Patents
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35525
PATENT TRADEMARK OFFICE
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REPLY BRIEF (37 C.F.R. 41.41)

This Reply Brief is submitted in response to the Examiner's Answer mailed on February 21, 2007.

No fees are believed to be required to file a Reply Brief. If any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447.

RESPONSE TO EXAMINER'S ANSWER

A. GROUND OF REJECTION 1 (Claims 1-5 and 8-25)

Claims 1-5 and 8-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Heisch (U.S. Patent No. 5,774,724).

A.1 Claims 1-5, 14-17 and 21-23

Claim 1 on appeal herein is reproduced below for the convenience of the Board:

> 1. A method in a data processing system for processing instructions, the method comprising:
>
> responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present; and
>
> forcing an interrupt if the performance indicator is present.

In the Appeal Brief filed October 24, 2006, Appellants asserted that Heisch does not disclose or suggest "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present" as recited in claim 1, and, therefore, does not anticipate claim 1.

As pointed out in the Appeal Brief, Heisch describes an instruction address breakpoint register (IABR or IAB register) that causes an instruction address breakpoint exception when an instruction at that address is executed. As described in Col. 5, lines 58-65 of Heisch:

> The basic operation of an IAB is as follows. First, an address of interest may be loaded into the IAB register, whereupon the microprocessor associated with the IABR executes program instructions while the register is monitored. The contents of the IAB register, more specifically, are compared to the address of the particular instruction executing at a given time. This function is shown by the IABR compare block **64** of FIG. 2. (Emphasis added.)

In Heisch, the contents of the IAB register are compared to an address of a particular instruction that is executing. Heisch does not determine whether a performance indicator is present that identifies that execution of an instruction is to be monitored in response to receiving the instruction for execution.

In rejecting the claims, the Examiner asserts that the act of matching the contents of the IABR to the executing instruction's address in Heisch constitutes a "performance indicator". In this regard, in Heisch, the IABR is monitored to determine if a preselected address stored in the IABR equals an address of an instruction currently to be executed. An interrupt is caused if there is such a match. In the Appeal Brief, Appellants pointed out that even if the match in Heisch is construed as comprising the performance indicator of claim 1 (which Appellants do not believe is a reasonable position), Heisch still does not anticipate claim 1.

In responding to Appellants' arguments presented in the Appeal Brief, the Examiner states:

> When making evaluations about a processing system, using every-day terminology like "identify" and relating it to a computer can often be rather difficult. The American Heritage Dictionary 4th Edition does not, as one might expect, have a "computer architecture" definition of the word "identify"; however, the first general definitions listed are "to recognize or establish as being a particular person or thing" and "verify the identity of."
>
> The first definition appears to clearly be in support of the current rejection. The performance indicator of Heisch (of which Appellant does not admit or deny the existence-see page 12 of the Appeal Brief) is only required to recognize the existence of performance monitoring or, as it relates to a processor, show that the existence of performance monitoring has some effect on the performance indicator. Here, this is clearly the case. As Applicant correctly describes in page 12 of the Appeal Brief, in Heisch "the IABR is monitored to determine if a preselected address stored in the IABR equals an address of an instruction currently to be executed. An interrupt is caused if there is such a match." Additionally, as described in the final Office Action on page 3, "The examiner asserts that matching the contents of the IABR register to the executing instruction's address constitutes a 'performance indicator'". Therefore, to satisfy the definition of "identify" it is simply required that the performance indicator recognize that such a match occurred and to act appropriately as a result (in the case of Heisch, by raising an interrupt as a result of such a match). By satisfying this definition, the rejection under Heisch correctly satisfies the "broadest reasonable interpretation" requirement of 35 U.S.C. 102.
>
> Appellant, based on the arguments presented, appears to desire that the definition of "identify" be narrowed. In particular, note the second definition given of identify: "verify the identity of". Appellant, it seems, believes that a definition, such as this one, implies a further requirement for identification-in particular, that the "thing" being identified cannot always exist. Examiner concedes that this second definition of "identify" does appear to carry that additional requirement.

> Despite the fact that the first definition of "identified" supports the current rejection (therefore, making it reasonably interpreted), a further analysis will be provided. Appellant states that, "In Heisch, all instructions are monitored and any 'indicator' that may be present in Heisch may indicate whether there is to be an interrupt, but does not indicate that execution of an instruction is to be monitored is present." This statement is false. All instructions in Heisch are not monitored. Monitoring is not always enabled. This is clear from the summary of Heisch, "By coupling the performance monitor and IABR functionality, the performance monitor may thereby be enabled and disabled on a per instruction address basis" (Heisch col4 lines 4-7).
>
> Therefore, the limitation in question is satisfied by Heisch based on two distinct definitions of "identifyr1-the satisfaction of either one of them making the rejection proper.

Examiner's Answer dated February 21, 2007, pages 13-14.

As confirmed in the above recitation, the Examiner attempts to read Heisch on claim 1 by asserting that the act of matching the contents of the IABR to the executing instructions address in Heisch corresponds to the performance indicator recited in claim 1. The Examiner also contends that the term "identifies" as used in claim 1 can be construed as meaning "to recognize or establish as being a particular person or thing." The Examiner then apparently concludes that the act of matching the contents of the IABR to the executing instruction is the same as recognizing that such a match occurred and acting appropriately as a result (in the case of Heisch, by raising an interrupt as a result of such a match).

Appellants respectfully disagree with the Examiner's analysis and conclusions. Consider first the second portion of the claimed limitation in claim 1 "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present." If, as the Examiner contends, the act of matching the contents of the IABR to the executing instructions address in Heisch corresponds to the performance indicator recited in claim 1, and, further, if the term "identifies" as used in the claim means that the match is recognized as existing, this line of reasoning still does not result in a teaching of a performance indicator that "identifies that execution of the instruction is to be monitored is present." The Examiner says that the term "identifies" in claim 1 is interpreted as corresponding to recognizing

that the match condition (performance indicator) exists. The claim, however, does not recite this. Instead, claim 1 clearly recites that the performance indicator identifies that "execution of the instruction is to be monitored", not that the performance indicator exists as suggested by the Examiner.

Furthermore, claim 1 also requires that a determination be made of whether a performance indicator that identifies that execution of the instruction is to be monitored is present. Inherently recognizing, in some manner, that a match condition exists when the match condition comes into existence, is not, in any way, a disclosure or teaching of "determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present" as recited in claim 1.

Accordingly, even accepting the Examiner's interpretation of Heisch, the reference still does not disclose or suggest "determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present."

Furthermore, Heisch also does not disclose or suggest the first portion of the claimed limitation: "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present". Nowhere does Heisch disclose or suggest that a determination of whether a match between the IABR contents and an executing instruction (the alleged performance indicator) is present is made in response to receiving an instruction for execution in an instruction cache in a processor in the data processing system.

In general, Appellants respectfully submit that even with the Examiner's rather convoluted and unreasonable interpretation of the disclosure in Heisch, Heisch still does not anticipate claim 1, and claim 1 patentably distinguishes over Heisch in its present form.

A.2 Claims 8-13, 18-20 and 24-25

Independent claim 8 is as follows:

> 8. A method in a data processing system for processing data, the method comprising:
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> responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present; and
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> generating an interrupt if the performance indicator is present.

As discussed in detail above with respect to claim 1, Heisch employs an IABR that stores preselected instruction address breakpoints and causes an interrupt whenever an address of an instruction currently to be executed matches a stored address. Even if matching of the contents of the IABR to the address in question could be construed as comprising a performance indicator as proposed by the Examiner, which, as indicated above, Appellants do not believe to be a reasonable position, Heisch still does not disclose or suggest "determining whether a performance indicator that identifies that access of the data is to be monitored is present" and does not disclose or suggest making such a determination "responsive to an access of data" as required by claim 8.

Claim 8, accordingly, is also not anticipated by Heisch and patentably distinguishes over Heisch in its present form.

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Respectfully submitted,

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